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Air Force CALS Test Network

VHSIC Hardware Description Language

Standard Compliance Test Planning Study

24 December 1993

Prepared for
Electronic Systems Center
Air Force CALS Program Office
HQ ESC/AV-2
4027 Colonel Glenn Hwy Suite 300
Dayton OH 45431-1672

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Prepared By
Air Force CALS Test Bed
Wright-Patterson AFB, OH 45433

AFCTB Contact
Gary Lammers
(513) 427-2295

AFCTN Contact
Mel Lammers
(513) 427-2295

Executive Summary

The VHSIC Hardware Description Language (VHDL) is an advanced hardware description language (HDL) that supports the design and documentation of digital systems. The Continuous Acquisition and Life-cycle Support (CALS) program has designated VHDL as a CALS "building block data format." The purpose of this study is to analyze the need for VHDL testing to support compliance to the VHDL Standard, and to determine appropriate Air Force CALS Test Bed (AFCTB) activities to support VHDL Standard application in the DoD.

VHDL is a recognized industry standard and is accepted by DoD and other Federal agencies. It enables designers to model, simulate, and test systems from requirements to detailed designs. Models are used directly to manufacture hardware. VHDL also completely documents digital designs in completely technology independent data that can be used to reprocure or retrofit systems long after an original integrated circuit technology is no longer available. VHDL data, used to reprocure and retrofit weapon system electronics, offers inestimable potential for life cycle savings as weapon life spans generations of technologies.

The design automation industry has and continues to develop numerous VHDL design and support tool developments. The electronic design industry is rapidly moving to VHDL. Several DoD programs, including the F-22, are using VHDL for digital system developments. Although there is an accepted industry standard, there is no test capability to assure the industry tools comply with the standard, or that VHDL data is in compliance. Therein lies a problem for the DoD. The DoD needs the assurance that acquired weapon system data will be usable for future reprocurements or redesigns. There is a need for VHDL tool compliance testing as well as VHDL data testing. The National Institute of Standards and Technology has responsibility for tool certification, but has not been able to develop the required test suite.

The industry consortium, VHDL International (VI), founded to promote VHDL as the standard worldwide language for the design of electronic systems, has initiated an effort to develop a VHDL tool test suite. Although it is using all of the DoD developed test resources, it does not appear that VI has fiscal resources to develop a test suite which will provide complete test coverage of the current ANSI/IEEE 1076 VHDL Standard. The VI initiative is the only currently ongoing effort to develop test tools required to verify or validate VHDL compliance.

Without compliance testing capabilities industry, as well as the DoD, cannot be assured of obtaining the full benefits of VHDL. The DoD has much to gain in full VHDL compliance and standardization because of the long service lifetime of its systems and the many reprocurements and redesigns that take place over typical weapon lifetimes. In order to achieve the full potential of VHDL in the development and support of digital electronic systems, it is essential that VHDL be consistently applied as a design and documentation standard throughout the industry.

VHSIC HARDWARE DESCRIPTION LANGUAGE STANDARD COMPLIANCE TEST PLANNING STUDY

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

Page

TABLE OF CONTENTS (Continued)

VHSIC HARDWARE DESCRIPTION LANGUAGE STANDARD COMPLIANCE TEST PLANNING STUDY

SECTION I

INTRODUCTION

The inexorable advance of very high speed integrated circuit (VHSIC) and very large scale integrated (VLSI) circuit technology has resulted in the mushrooming complexity of digital electronic systems. This burgeoning complexity of electronic design, and the pressure to decrease its development time and cost, have led to a new approach to electronic design. Circuit designers have developed modeling and simulation techniques to validate their designs before they commit the designs to hardware development. As a result several hardware description languages and a number of simulation software packages have been developed and marketed in an expanded electronic design automation (EDA) industry.

The VHSIC Hardware Description Language (VHDL) is the newest and most comprehensive of the hardware description languages (HDLs) in use today in the EDA industry. VHDL enables designers to model, simulate, and test designs at all levels of architecture, from top-level system descriptions down to the gate level. High level architecture models document system requirements. The lowest level, gate level models are used directly by the integrated circuit manufacturing process to produce the designed hardware. VHDL models include test information that is used during the design processes to validate the designs. Models at all levels are machine simulatable permitting validation of each design step. The test data used in the design process can also be applied in developing automatic test programs for operational hardware diagnostic testing. VHDL is a recognized industry standard, and is an adopted Federal standard.

In addition to VHDL's unique ability to support the VHSIC and VLSI design environments, the VHDL language completely documents the design of digital electronic entities at every design level at which it is applied, i.e., at the abstract digital system and subsystem architectural levels, to the register transfer logic (RTL) and gate levels of circuit design. VHDL models provide the capability to model digital systems in a completely technology independent manner. This feature provides for technology transparent, non-perishable documentation that can be used to reprocure or retrofit systems long after an original integrated circuit technology has become obsolete and is no longer available from industry.

The application of VHDL offers great potential for weapon system life cycle cost savings. System acquisition development can be accomplished quicker and at less cost using VHDL modeling and simulation. VHDL technology transparent documentation, used to reprocure and retrofit weapon system electronics, offers an inestimable potential for life cycle savings as weapon life spans generations of technology change.

1.1 Purpose

The purpose of this study is to analyze the need and document the requirements for VHDL testing to support VHDL standard compliance, and to determine appropriate Air Force CALS Test Bed (AFCTB) activities to support VHDL Standard application in the DoD.

CALS Program guidance designates VHDL as a CALS "building block data format." This digital electronic design and documentation tool does not have the same status in CALS as the standards for textual and graphics data. The CALS test and support activities, including the AFCTB, are not involved in VHDL testing, or in VHDL technical support, as they are with the other CALS standards for automated data interchange.

The CALS Program currently supports some VHDL related efforts. At this time, when industry is moving towards wider application of VHDL and there is official DoD "encouragement" to apply VHDL, it is appropriate that the CALS Program evaluate its position with respect to additional support of VHDL. Thus, AFCTB management directed this VHDL study to examine VHDL testing needs.

1.2 Scope

The study examines the background and development of VHDL and its current support by industry, the DoD and other Federal agencies. The study documents VHDL data testing and tool testing requirements, and the resources required to perform these testing activities.

The study examines in detail the current state of development of a "VHDL tool test suite." This is a required resource to test, validate, and certify VHDL tools as conforming to the VHDL Standard.

The study documents the capabilities of candidate organizations, including the AFCTB, that could perform VHDL testing. The study closes with a summary of finding and conclusions, and recommends support for the development of VHDL tool testing capabilities.

1.3 VHDL Description

VHDL is a design and documentation language used to develop digital electronic systems. It creates descriptions of electronic structures at the component, board, and system level. In addition to supporting documentation, VHDL also supports design verification through simulation, and design creation through synthesis, enabling designers to rapidly perform what-if analysis to select the most appropriate design solution. VHDL was developed to support the DoD VHSIC program requirements to model and document digital electronic systems. It is both a design tool and a documentation tool.

VHDL makes no assumptions about the technology of a device or the methodology used to design a device. An abstraction of the nature of digital hardware devices is used as the basis of the language and includes behavioral, timing and structural characteristics of digital devices.

The general model, on which VHDL is based, consists of three interdependent models: a behavioral model; a timing model; and a structural model, such as a netlist. In addition each VHDL model includes a test model, i.e., stimuli (test vectors) to test the model.

1.3.1 VHDL -- A Design Language

Although it is the newest HDL, VHDL is recognized and widely used as a design language. It is a leading edge technology design language. It was developed to enable designers to implement the advanced VHSIC technology. It is being applied across both the DoD VHSIC and the industry developed VLSI circuit design arenas. VHDL can be used with many types of design tools, i.e., model simulators, circuit synthesizers, silicon compilers, placement and wiring tools, test generators, architectural specification and analysis tools, and timing analyzers. Its application as a design tool is encouraged by an Air Force acquisition policy letter and its use is required in DoD system acquisitions by a military standard.

Traditionally, electronic design has been performed at the gate-level using standard off the shelf components. With the application of VHSIC and VLSI circuit technologies, hardware design complexity has grown by orders of magnitude. The building blocks in typical systems are now microprocessors or application specific integrated circuits (ASICs) which represent thousands of gates in complexity. Bottom-up design methodologies are giving way to hierarchical design practices, making management of this technology possible. VHDL is a hierarchical hardware description language which lends to this design process. By using VHDL as a specification tool, simulation of complex systems can begin before implementation details are fully specified.

VHDL can be used to model the range from high level architectural descriptions to gate level descriptions. The language is hierarchical and mixed-level simulation is supported. The concepts embodied in the language's timing model mirror real hardware--the VHDL models of designs behave like real hardware. Other languages cover only subsets of the capabilities of VHDL. None are as comprehensive.

A major power of VHDL is that it is a standard, recognized by several standardization organizations and maintained by an international professional organization. VHDL is recognized and is gaining wide acceptance throughout industry. VHDL support tool development is rapidly overtaking the total support development for all other HDLs. With VHDL as the standard, industry can more easily communicate designs among participants in a design process. VHDL provides designers the capability to describe the concepts they are developing and utilize these descriptions with tools in a way that simplifies the design process.

1.3.2 VHDL -- A Documentation Language

VHDL is a descriptive language, one that is both human and machine readable. VHDL models completely document the digital hardware design. Top level design models describe the essence of system requirements. Lower level models, derived from the top-level documentation, are used directly in the production of digital integrated circuit devices.

At high levels of abstraction, the language makes an excellent specification medium for future designs to be created in new technologies or with alternative architectures. At lower levels of abstraction, the language serves well as a specification of what is to be fabricated. Low level VHDL models are used as inputs to the manufacturing process of integrated circuits, and the development of circuit testing data.

VHDL models can be defined in a technology transparent manner that permits these models to be developed in different circuit realization technologies. Thus at some future time, VHDL models that have been preserved can be used to develop the original designed functions in a subsequent technology, different from the one in which the original functional devices were developed. This capability of VHDL can drastically reduce future system support costs. VHDL documentation can eliminate the expensive re-engineering of systems, subsystems and components currently required to reprocure and retrofit replacements for outdated technology. This capability makes VHDL documentation an invaluable asset for DoD systems that will be maintained long after their original technologies become obsolete.

In summary, VHDL supports the development, verification, synthesis, and testing of digital hardware designs at all levels of the design process. VHDL models also support the manufacture of digital circuits and components. VHDL models completely document the system design process and provide a vehicle to communicate hardware design data for initial procurement, maintenance, modification, and reprocurement of hardware over the entire life of digital systems.

1.4 VHDL -- A CALS Standard

The Continuous Acquisition and Life-cycle Support (CALS) Program strategy is the development of an integrated data environment for the functional exchange of business and technical information between DoD and its industrial base. CALS and Electronic Data Interchange (EDI) emphasizes that information about the design, use, and support of a product must be captured as soon as it is available.

As a digital electronic system design language that completely documents the development of a major aspect of weapon systems--digital electronics--VHDL is a vital component to the CALS and EDI strategies. The CALS program has made VHDL a component of its structure; however, because VHDL is a relatively recent addition to a specialized documentation area, it has not received the attention in the CALS Program that the other standards receive. This report provides a basis for the CALS Program to develop a greater support emphasis for the VHDL Standard.

SECTION II

BACKGROUND

This section contains a discussion of the requirement for hardware description languages, the development of VHDL, and its standardization. This is followed by a survey of the current directives associated with the use of VHDL, current DoD VHDL applications, CALS Program support of VHDL, and other VHDL related activities outside of the testing area.

2.1 Hardware Description Languages

With the development of VLSI circuits, a structured design process is required. In response to this need, considerable effort has been and is being invested in the development and application of design aids. HDLs are specific examples and have been in use for over a dozen years. Early languages did not have the capability to model with a high degree of accuracy, and their language constructs served only limited hardware structures. More recently, HDLs have been developed with more precise timing and broader application capabilities.

Hardware description languages provide two functions in the design process: modeling and documenting a design. Precise documentation ensures design accuracy and is important in providing for design portability. HDLs are supported by simulation software and HDL models of systems are simulated to validate their designs. Prototyping of complicated systems is extremely expensive. The goal of those who develop HDLs is to replace the prototyping process with validation through simulation. HDL models and data are also used for generating automatic test programs and for silicon compilation, i.e., the physical circuit manufacturing processes.

Today's high-level design automation environment combines hardware description languages, design and test synthesis, and system simulation to provide complete functional representation of an integrated circuit before a design is committed to silicon.

2.2 VHDL Development

The DoD sponsored the development of the VHDL, beginning in 1983. Three major contractors contributed to this development, IBM, Texas Instruments, and Intermetrics. The original intent of the language was to serve as a means of communicating designs from one contractor to another in the VHSIC program. However, its application has been broadened and the design of the language has received input from many individuals in the EDA and computer industries, and thus reflects a consensus of opinion as to what characteristics a hardware description language should have.

In August 1985, version 7.2 of the language was released, representing the completion of the first major stage of the language development. This version was a complete comprehensive

language specification. It provided constructs for both structural and behavioral modeling to support simulation, and provided a means to document digital designs. At this point, the VHSIC Program turned over the language specification development to the Institute of Electrical and Electronic Engineers (IEEE).

2.3 VHDL Standard Development

The IEEE undertook a review of the VHDL development with the ultimate goal being the development of an improved, standard version of the language. The review was accomplished by the VHDL Analysis and Standardization Group (VASG), a working group within the Design Automation Standards Subcommittee (DASS) of the Computer Society of the IEEE. The work of the VASG was also jointly supported by the Automatic Test Program Generation Subcommittee of the IEEE Standards Coordinating Committee 20. In order to assist the voluntary standardization process of the IEEE, the Air Force Wright Aeronautical Laboratories contracted with CAD Language Systems Inc., to support the analysis and final definition of the standard.

The IEEE enhanced the language substantially to meet its goal to develop a production quality language suitable as a design tool to be used throughout the design cycle. Industry representation from both EDA vendors and users had a major input to the IEEE review. In June 1987, the IEEE standards board accepted the revised and much improved version of VHDL as a standard. The standard was officially released in December 1987 as the IEEE 1076-1987 Standard VHDL Language Reference Manual (LRM). The main purpose of the LRM is to define the language accurately. Its primary audiences are the implementor of tools supporting the language and the advanced users of the language. The LRM provides the tool builder with specific, unambiguous rules of how VHDL-compliant tools must behave.

In addition to the IEEE endorsement of VHDL, the American National Standards Institute (ANSI) also has recognized the language standard. The standard is currently known as ANSI/IEEE 1076-1987 VHSIC Hardware Description Language.

IEEE standards undergo periodic formal review. The VASG begin a review of the VHDL standard in 1990. This has been a major effort in that several areas not treated in the initial standard are being added. One important aspect of the update is the addition of language rules to better support digital circuit synthesis. The update effort was completed and the final approval balloting process has been completed, however the update has not been published as yet.

2.4 VHDL Application Direction and Guidance

Direction and guidance for the required and recommended application of VHDL is referenced in Government documents summarized in the following paragraphs.

2.4.1 MIL-STD-454N

MIL-STD-454N, Standard General Requirements for Electronic Equipment, is the technical baseline for the design and construction of electronic equipment for the Department of Defense. The document contains 76 separate requirements, covering the common requirements to be used in military specifications for electronic equipment. In applying this standard, each requirement applicable to a specific specification is to be individually referenced.

The standard addresses VHDL in Requirement 64, Microelectronic Devices. This requirement establishes criteria for the selection and application of microelectronic devices based on the objectives of achieving technology superiority, quality, reliability, and maintainability in military systems. Requirement 64 directs VHDL application as follows:

> Digital application-specific integrated circuits (ASICs) designed after 30 September 1988 shall be documented by means of behavioral VHDL descriptions in accordance with ANSI/IEEE 1076.
>
> Digital qualified devices for use in board level designs after 30 December 1991 shall be documented by means of behavioral VHDL descriptions in accordance with ANSI/IEEE 1076.
>
> Digital ASICs designed after 31 December 1991 shall have all test vectors and test waveforms documented and delivered to the Government in the Waveform and Vector Exchange Standard (WAVES). (Note: WAVES data is derived from VHDL model data and supports the efficient development and documentation of automatic test program sets for digital hardware maintenance and support.)

2.4.2 DID DI-EGDS-80811

Data item description (DID) DI-EGDS-80811, VHSIC Hardware Description Language (VHDL) Documentation, was developed to detail unique contract requirements for VHDL model documentation. The DID references the IEEE Standard VHDL Language Reference Manual, IEEE Std 1076-1987.

The DID lists specific VHDL documentation content: model hierarchy and entity requirements, structural and behavioral body requirements, and simulation support. Detailed VHDL documentation (file) format and delivery instructions are also specified.

The DID states the preferred documentation shall be composed of nine-track magnetic tape records, similar to MIL-STD-1840 requirements, but does not reference MIL-STD-1840.

2.4.3 MIL-STD-1840B

MIL-STD-1840B, Automated Interchange of Technical Information, is the CALS digital format standard. It standardizes formats for exchange of digital information necessary for the development and logistic support of defense systems between organizations or systems.

The document references IEEE 1076 Standard VHDL, and requires VHDL electronic application data files be delivered in accordance with the VHDL product description and file format standard as defined in the IEEE 1076 Standard.

2.4.4 USAF Acquisition Policy 92M-017

This memorandum, subject, "Software Intensive Hardware Risk Reduction - Action Memorandum," was issued 17 February 1993 by the Office of the Assistant Secretary, Department of the Air Force. It noted the following:

> "The DoD Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL), ANSI/IEEE 1076, along with the commercial availability of design, analysis, and simulation tools, provide for simulation of product design before build. The use of simulation as part of a disciplined structured engineering process can significantly reduce risk and cost associated with front-end design and analysis of digital systems."
>
> "System program offices will encourage contractors to utilize VHDL to simulate design of digital systems (processors and other digital equipment) before building hardware, and will develop contractual vehicles that motivate contractors to utilize appropriate tools as a part of their risk/cost management approach."

2.4.5 FIPS PUB 172

The Department of Commerce (DoC), National Institute of Standards and Technology (NIST) announced adoption of ANSI/IEEE 1076-1987 Standard VHDL, as a Federal Information Processing Standard (FIPS) in FIPS Publication (PUB) 172, 29 June 1992. FIPS PUBs provide Federal standards for high level digital design information and documentation languages. Among the stated objectives of the VHDL Standard are to: (1) reduce costs through increased design productivity and accuracy, and by insuring that design skills are transportable, (2) reduce digital system life cycle costs by establishing a common documentation language to transfer design information across organizational boundaries, and (3) protect the investment of digital hardware from obsolescence by insuring subsequent standard revisions are compatible with the superseded versions.

The NIST VHDL FIPS PUB 172 states that attainment of these objectives depends upon the widespread availability and use of comprehensive and precise standard language specifications.

The standard is to be applied for design and documentation of digital systems where (1) the digital system will need to be maintained and upgraded, and (2) it is required to have the design understood by multiple people, groups, or organizations. The VHDL FIPS PUB states three implementation areas of consideration: acquisition of VHDL processors, interpretation of FIPS VHDL, and validation of VHDL processors. These are summarized in the following three paragraphs.

VHDL processors, acquired after December 1992 to be used in digital designs with Federal applications, should implement FIPS VHDL. A twelve month transition period, ending December 1993, was provided for industry to produce VHDL processors conforming to the standard.

The National Institute of Standards and Technology will provide for the resolution of questions regarding the specifications and requirements, and issues official interpretation as needed.

The validation of VHDL processors for conformance to the standard applies when NIST VHDL processors are available. NIST does not have procedures for validating VHDL processors at the present time and is investigating methods to validate processors for conformance to the standard.

2.4.6 MIL-HDBK-59B

Military Handbook 59B, "DoD CALS Implementation Guide," provides the "umbrella" guidance for applying the CALS strategy to the acquisition, management, and use of digital data in support of defense systems. Several process improvements and benefits are to accrue from the implementation of the CALS strategy. VHDL directly supports two of these improvements and benefits: (1) VHDL supports "improved information quality for equipment design and acquisition, support planning, and re-procurement and maintenance through direct coupling of design processes and integrated databases," and (2) VHDL supports "a more responsive industrial base through development of integrated design and manufacturing capabilities and industry networks to build and support hardware based on digital product descriptions." (The quotes indicate the CALS improvements and benefits.)

The handbook makes a distinction between the four CALS MIL-SPEC data format specifications and the VHDL Standard. VHDL is described in a category, "other digital data interchange standards" that "may be useful in exchanging specific types of data in digital format." VHDL is described in the handbook as follows:

> "VHDL is a formal notation intended for use in all phases of the creation of electronic systems. Because it is both machine and human readable, it supports the development, verification, synthesis, and testing of hardware designs, the communication of hardware design data, and the maintenance, modification and procurement of hardware."

The handbook also sets forth responsibilities for development, validation and maintenance of standards and specifications as follows: The CALS Program Office is to develop standards and facilitate accelerated CALS implementation within industry. NIST is to assist in the development and maintenance of CALS standards and specifications. The CALS Test Network (CTN) is to validate digital data formats.

2.5 Current VHDL Applications in the DoD

The VHDL Standard was issued in 1987; however, mandates within DoD standards and top-level encouragements to apply VHDL have appeared only in the last few years. Thus, VHDL is just beginning to be broadly applied in DoD weapon system acquisition and support. In spite of being developed by the DoD, commercial interest and application has actually been more intense than in the services.

VHDL is being applied in the acquisition development of new weapon systems and in the support of operational weapon systems. Representative applications reviewed in this study are described. They indicate the breadth of VHDL applications that will occur in subsequent years. One of the first acquisition programs to use VHDL was the Air Force F-22 program. This application is discussed in paragraph 2.5.1. VHDL is also being used in the upgrade and reprocurement of components and subsystems of operational weapon systems. Examples of these applications are described in paragraph 2.5.2.

2.5.1 System Acquisition Applications

Several DoD system acquisitions are applying VHDL in the development of digital electronics. Included are three Air Force programs, the F-22 Advanced Tactical Fighter (ATF), the Advanced Spaceborne Computer Module (ASCM), and the Forward Electronic Warning System (FEWS). The Army Light Helicopter (LH) program is following the F-22 with VHDL since its conceptual development involved the common avionics baseline.

The F-22 Advanced Tactical Fighter acquisition development has forged new ground in the application of VHDL. VHDL is being used to meet the two basic needs previously described, design simulation and support documentation. The following paragraphs describe how these needs are being met by the application of VHDL.

2.5.1.1 F-22 Program Requirements

Design simulation and verification is required to efficiently conduct modern system development because of the complexity of electronic systems brought about by the increasingly dense integrated circuit technology. Prior to the F-22 initial conception phase, experience indicated that 50 percent of electronic devices, developed without simulation, had to be redesigned because of interface related problems found later in the course of development. F-22 engineering management realized that, in order to successfully meet the challenges of their complex system development, verification of the avionics designs was necessary before

the designs were developed in hardware. The F-22 Program made a commitment to model and simulate designs in order to avoid costly and time-consuming design rework.

The F-22 program required a high level system design language, i.e., a simulatable hardware description language to simulate system elements and interfaces and verify their operation before the elements were built. Contractors developing portions of common systems needed to have a common understanding of subsystem functional requirements and to precisely share design interfaces. There was a need to be able to exchange this design information across the F-22 multiple-vendor environment. (There are 20 vendors and designers involved in the F-22 avionics development.) The major developers also needed to be able to precisely simulate their own designs, along with the designs of other developers and vendors, to verify functional designs and compatibility of interfaces.

The F-22 program management understood that paper documentation would not be adequate to meet the size and complexity of the their avionics system, and in addition, they were concerned about support of follow-on maintenance. Reconstructing the intended behavior of components to be replaced, as it is now done from paper documentation of current weapon systems, is costly now and would be totally unsatisfactory for the complex F-22 avionics system. Future design and integration of system upgrades (required to meet new threats, new mission capabilities, or take advantage of advances in technology) will require the same capability used in the development of the original system. A means to obtain and maintain correct, as built, documentation was needed that would support future system modifications as well as future re-procurement of current functional "parts." In summary, the F-22 avionics needed a simulatable HDL that would also preserve the design documentation in a standardized form, usable for future support needs.

2.5.1.2 F-22 VHDL Application

The F-22 program elected to use VHDL and to pursue a rigorous process of system modeling and simulation prior to committing to hardware development. The process has a dual focus: (1) to provide a design approach that reduces risk, and (2) to provide "as built" reprocurement documentation. Despite its immaturity, VHDL was selected for the F-22 avionics development. VHDL was selected because it uniquely met the broad requirements of the dual focus, and it offers the promise of continuing standardization that will preserve the usefulness of the current developed documentation for future applications in reprocurement and system upgrade.

When the F-22 Program selected VHDL, there were no validated VHDL tools to support transportability of models between various tools used by different subsystem designers. There are only a few simulators that meet all (or most) of the VHDL Standard's requirements. However, among these simulators, different interpretations of the language rules can cause models that run on one simulator be incompatible with other simulators. Differences and inconsistencies exist in the VHDL simulators (the major VHDL design tool) used by the 20 avionics developers and vendors.

A work-around was devised and is employed to mitigate the language interpretation differences, modeling differences, and simulation inconsistencies of different simulators and other tools used by the F-22 vendors. All models, from the various developers and vendors, are made to conform to the characteristics and requirements of three top-of-the-line simulators, specified by the F-22 Program. In order to pass this conformance process, each model must run and provide the same results on all three simulators. Models that do not run on all three simulators are re-designed to accommodate all of the simulator requirements, but still model the original intended functional design. This, in effect, forces all model designers and developers to conform to a "common" VHDL language, which is defined by the logical intersection of the language characteristics of the three VHDL simulators specified by the F-22 Program.

2.5.1.3 F-22 System Simulation Process

The implementation of VHDL in the F-22 Program is part of a rigorous top down system simulation (TDSS) process. TDSS standards and practices, including an F-22 VHDL Model Specification document based on the VHDL data item description (DID DI-EGDS-80811), were developed and are applied uniformly across all vendors. Each contractor involved in a common F-22 component development or common interface is required to follow TDSS documentation and test plans. Specifications and tests are cross-referenced to common components and interface specifications. Test plans and model specifications are shared electronically among the contractors.

F-22 avionics systems developers are required to design and test their system, subsystem and component models, at various levels of design, to verify critical functions and interfaces before key program development milestones, i.e., preliminary design review and critical design review. The simulations verify the designs at each stage and expose specification misinterpretations and/or ambiguities prior to large resource investments.

High level behavioral model test results are required to be delivered and approved before lower level design is initiated. Only after the successful development and testing of the gate level models are the designs committed to fabrication. All VHDL designs are finally verified by hardware. Some developers use VHDL synthesis tools to move from the register transfer model to hardware design, automating this step. All VHDL code, including the top level behavioral models, becomes part of the design documentation to be maintained and used for future reprocurement or design modification.

2.5.1.4 F-22 Application Observations

F-22 Program Office engineering staff believe that without externally imposed validation requirements, to encourage or force compliance with the VHDL standard, vendors will continue to maintain their differences in VHDL language interpretation and model/tool inconsistencies. Each simulator's unique capabilities provide distinctive marketing points in today's competitive design automation industry.

In addition to the simulator (language) differences, three other observations and concerns have come from the F-22 VHDL experience. First, inconsistent modeling (language interpretation) throughout the automated design industry results in non-standard ASIC models and incompatible "standard part" model libraries. The issue of model libraries raises the question of the need for a government agency model library to support a "standard parts" program in order to support digital system design and acquisition.

Secondly, synthesis tools are not as mature as simulators. Various synthesis tools provide only a degree of automated development of lower (gate-level) models from the higher level architecture models. The VHDL Standard upgrade will support additional development of "standardized" synthesis tools. (Reference paragraph 2.3.)

The third concern is the development of automatic test system (ATS) programs from VHDL model data. The F-22 development statement of work (SOW) specified the development of WAVES data for ATS test program set (TPS) development. However, the process of VHDL model to WAVES data conversion is not fully developed, and the fully automated TPS development can not be realized now.

2.5.2 System Support Applications

The Sacramento Air Logistics Center (SM-ALC) Advanced Electronics Technology Group (AETG) is responsible for advanced microelectronics, electronics logistic retrofit engineering, and VHDL application support across the Air Force. The AETG has developed and implemented VHDL supported retrofit engineering techniques for prototyping the design of components and subsystems, to replace obsolete and no longer available items.

2.5.2.1 VHDL Reverse Synthesis

The AETG developed and applied VHDL reverse synthesis techniques for the design and production of replacement digital integrated circuit subsystems for the F-111 Digital Signal Transfer Unit and for the B-52 Electro-Optical Viewing System. In each case the replacement of subsystem components performing digital functions was required, and because of technology obsolescence, the original components could not be reprocured. VHDL was used in these efforts to model the functional characteristics of the component or subsystem being replaced. These models were simulated to "test" if they behaved like the original parts. Following successful simulations, the models were used to design the new subsystems and subsystem components in current digital technology. Finally, new component and circuit board subsystems were developed and tested to determine if the new part would functionally replace the original.

SM-ALC currently supports three other VHDL related retrofit projects. Two programs involve a reverse synthesis retrofit design for an Army weapon system and a top-down VHDL design for the B-52 Fiber-Optic Interphone System. In addition AETG conducted a US Air Force--United Kingdom (UK) Royal Air Force (RAF) VHDL cooperative demonstration. This is described in the following paragraph.

2.5.2.2 VHDL Demonstration

The AETG carried out a cooperative demonstration with the RAF to demonstrate two aspects of VHDL application in the existing logistical and maintenance infrastructures of the two countries: (1) VHDL's capability to specify and support the manufacturing of a physical device independent of a specified technology, and (2) VHDL's portability to transfer the product package for manufacturing. The demonstration involved the reverse engineering and top-down VHDL design of an RAF aircraft circuit board subsystem configuration by the AETG, and the digital transfer of design information to a UK contractor with no prior VHDL associated manufacturing experience.

The new design, to be successful, was to emulate the original circuit board functionality and be compatible with the existing support infrastructure or test procedures. The demonstration was completed and the new board was successfully tested by the RAF, demonstrating portability of VHDL and its ability to completely model a complex hardware module.

2.5.3 VHDL Model Library

The Defense Electronics Supply Center (DESC) is developing a VHDL model library in response to the Defense Logistics Agency (DLA) CALS office requirements. It is to be a repository for VHDL models of digital electronic components--ASICs and other qualified devices for on-board design--developed by the DoD services. The archived models will retain and provide information for future component reprocurement. The component models will also be available to "re-use" in other system designs.

The repository will maintain two separate model libraries. One library will contain "proprietary" models, those that are developed and paid for by Government contract. The proprietary library will be accessible only by Government agencies or their designated contractors.

A separate library will contain "public domain" models--models of standard of-the-shelf components. These device models exist throughout the component design community, in vendor proprietary and other private libraries. Access fees to these libraries are high and there is no standardization among the various libraries. This motivates the DESC initiative to establish a library of public domain devices that have been designed into Government developed systems.

DESC is tasked to accept all component models delivered under DoD contracts. DESC will assure the models are accurate models, corresponding to the components which are in the systems delivered to the government. In addition, DESC is also developing the capability to validate model conformance to the VHDL Standard, insofar as is possible at this time without validated tools, and verify that the models are "good" models, viable for use in a future reprocurement or reuse in a new application.

The DESC model library project is ready to accept, verify, simulate, and store microelectronic circuit models. Currently the number of models being developed is small; only a few programs have contracts that require delivery of VHDL component models. However, it is anticipated that the volume of models to be archived will increase, in the near future, as VHDL requirements are placed on acquisition and support programs.

2.6 VHDL in the Commercial Market

There is a growing acceptance and use of VHDL in commercial applications. Of all of the HDLs, VHDL's popularity is the fastest growing at this time. Based on generally available market data, the VHDL market share is expected to increase from 44 percent of the installed HDL seats (tools applied) in 1991 to 65 percent in 1994. To have reached 44 percent level in 1991, when the language was only introduced in 1985, and the Standard published in 1987, indicates its rapid acceptance and use in the civilian sector. It is recognized for its power in the design of complex systems where its high level description capability excels, and for its ability to directly apply high level descriptions to the development of lower level, more detailed design data, down to the physical manufacturing processes and to product testing.

In the commercial environment, industry's ready acceptance of VHDL tools that may not conform exactly to the VHDL Standard may be due, in part, to the more isolated commercial design environment. Here designs stay within a single company or company sector and are less likely to have to be shared among dissimilar VHDL tool sets. Additionally, commercial systems have shorter lifetimes over which they must be maintained. When they are "reprocured" or upgraded, this is done by the same organization that did the initial development.

2.7 VHDL Infrastructure and Support

The DoD VHDL program infrastructure that supported the development of the VHDL language, and to a great extent the VHDL Standard, is largely absent today. This was a research and development (R&D) laboratory program, and as the VHDL "technology" matured, it has "transitioned" to the applications environment. However, VHDL is different than the usual technology developed in the laboratories. Unlike most laboratory developed technologies, VHDL continues to require an infrastructure for its support and maintenance. Four sources that partially provide this support to the VHDL application environment are described below.

First, DoD laboratories that developed VHDL continue R&D activities to further enhance VHDL and initiate related research projects. This is discussed in paragraph 2.7.1 below. In addition there are key DoD laboratory technical managers who continue to advocate the use and assist in the application of VHDL. They also lobby support for non-R&D work that needs to be completed to fully support VHDL. The prime example of work that needs to be done is the development of a VHDL tool verification capability. The influence of these personalities continues to be an influence to the earliest complete realization of VHDL's potential to the electronics design automation arena, and system acquisition and support arenas.

Secondly, the IEEE and its members provide a supporting infrastructure to the "operational" VHDL, i.e., the ANSI/IEEE 1076 VHDL Standard. The VASG, a working group within the Design Automation Technical Committee of the Computer Society of the IEEE, is responsible for the technical maintenance of the standard. They resolve issues that may arise with the language, and consider potential extensions to the language. The standard must be maintained so that "upward compatibility" results. Subsequent versions of the Standard must be compatible with the superseded versions in order for tools, developed in accordance with later versions, to accept models developed in accordance with earlier versions of the Standard. (Reference paragraph 2.4.5.)

Members of the IEEE committees serve in a voluntary capacity. Because of this, some of the work that these committees need to do must be supported by outside sources. The Air Force has provided contractor support assistance to the VASG and DASS as they developed the initial VHDL standard in 1987, and more recently as the standard was upgraded by the IEEE. Reference paragraph 2.3.

Thirdly, an industry consortium, VHDL International, currently proactively promotes and supports the VHDL Standard. This effort is discussed beginning in paragraph 3.4.

Finally, the DoD CALS Program, the individual DoD Services and the Department of Commerce (DoC) provide support to the application of VHDL. The DoC support is discussed in paragraph 3.3. The CALS support is described in paragraph 2.7.2.

The spectrum for future VHDL related developments is broad. Ongoing research is described in paragraph 2.7.1 below. However, at this time the challenge is to apply the standard consistently. The application of VHDL offers major opportunities for cost savings. The challenge is to facilitate and encourage proper and precise implementations of the VHDL Standard.

2.7.1 Laboratory Research Associated with VHDL

VHDL was developed as a part of the DoD VHSIC Program. Most of this development was directed by what is now the Electronic Technology Division, Wright Aeronautical Laboratory. Research in associated areas continues in the Air Force Materiel Command laboratories.

The ManTech Division of the Wright Aeronautical Laboratory is pursuing a project, Continuous Electronics Enhancement Using Simulatable Specifications (CEENSS) which applies VHDL modeling to specification development and documentation.

Recently an effort was undertaken by Rome Laboratory to develop an analog hardware description language (AHDL). As indicated earlier, work is not complete in providing a continuous processing thread from high level electronic models, to manufacturing, to test. Additional developments of the Tester Independent Software Support System (TISSS) and WAVES programs are also ongoing at Rome Laboratory.

2.7.2 Current CALS VHDL Support

This section describes current CALS activities that support the application of VHDL. All of these efforts noted in this study are supported directly or indirectly through the Air Force CALS Program Office.

2.7.2.1 Air Force CALS Program Office

In its effort to enable more effective generation, exchange, management, and use of digital data supporting defense systems, the CALS program has focused on moving from manual, paper-intensive defense system operations to integrated, automated processes. However, for the most part, current CALS data initiatives address standardizing the exchange of conventional documentation, i.e., text, graphics, etc. There has been little effort in fostering standardization of data in the electronic design automation field.

Air Force CALS Program Office management recognizes the significance of VHDL and its relevance to the CALS program objectives. The language couples the electronics design, manufacturing, and documentation processes, thus embodying the CALS goals of process improvement, integration, and automation. VHDL uniquely supports digital electronic system acquisition design, maintenance support, and re-procurement of digital systems and components. Its use can reduce acquisition and support costs by eliminating duplicative manual processes.

The AF CALS Program Office provides funding to the Air Force VHDL Program Office (AFVPO), supporting several VHDL initiatives. These are described in paragraph 2.7.2.2. In addition, this study is sponsored by the AFCTB. The AFCTB is a possible resource for VHDL testing.

2.7.2.2 Air Force VHDL Program Office

The AFVPO is part of the SM-ALC AETG. In addition to its VHDL activities the AETG has mission responsibilities in the areas of advanced microelectronics and logistics retrofit engineering. The VHDL tasks are mutually complementary with these AETG mission responsibilities. The AFVPO task activities are briefly described.

The AFVPO functions as tri-service focal point for the development of VHDL education and training resources and the promotion of the VHDL design methodology. A formal course targeted for engineering support organizations was recently developed with Army, Navy, and Air Force technical support.

The AFVPO supports and coordinates Government and industry VHDL development efforts and methodology demonstrations, which directly complement the AETG logistics retrofit engineering mission. VHDL modeling and simulation techniques have been used successfully

on several operational system electronic subsystem retrofit tasks, and have validated VHDL for systems support (Reference paragraph 2.5.2).

The AFVPO coordinates and supports efforts to formalize Government endorsement and support of the VHDL standard. Support is provided to NIST to update the VHDL FIPS PUB to align it to the recent IEEE VHDL Standard upgrade. The AFVPO monitors the VHDL International consortium initiatives and plans to support the consortium's development of the VHDL validation suite.

The AFVPO has assisted the establishment of a VHDL model library at the DESC (Reference 2.5.3). The AFVPO is coordinating and assisting in developing a model validation process for the DESC.

2.7.2.3 Air Force CALS Test Bed

The AFCTB, part of the Air Force CALS Program Office, provides testing and consultation to Government and industry organizations in the application of CALS standards. Organizations submit their CALS data to the AFCTB for evaluation. AFCTB developed test tools and products are used to evaluate data against the CALS standards. Test result feedback and assistance is provided to submitters to assist in developing CALS compliant capabilities.

There are no recognized VHDL testing capabilities in existence today. Commercial vendors supply VHDL tools that are advertised as VHDL tools, but there is no validation capability to assure these tools comply with the VHDL Standard. VHDL data developed by designers using various tools may not conform to the requirements of the VHDL Standard and thus may not be transportable to other VHDL tools. Since there are no validated VHDL tools, there are no test resources to determine if VHDL data complies with the VHDL Standard. Recognizing the need for VHDL testing, the AFCTB initiated this study to determine if the AFCTB should be involved in testing associated with the applications of the VHDL standard.

SECTION III

REQUIREMENTS AND RESPONSIBILITIES FOR VHDL COMPLIANCE TESTING

There are two areas of compliance with respect to the VHDL Standard. The first is VHDL model compliance, meaning models are structured in accordance with the VHDL Standard. The second area is VHDL tool compliance. Compliant VHDL tools support the development of compliant models, i.e., they correctly process VHDL Standard compliant model code and reject code which does not comply with the Standard. This section discusses the need for compliance in these areas and the organizations that have responsibilities to assure VHDL compliance.

3.1 VHDL Model Data Compliance

VHDL models serve a dual purpose in the systems acquisition/engineering development process. They are intrinsic to the design process of large digital systems. They embody the design entity, i.e., the digital component, subsystem, or system, in a machine executable and simulatable language or code. VHDL models are hierachical, ranging in levels from high level system requirement models to the lowest gate level models as the design progresses. VHDL gate level models are applied directly to the manufacturing process of the final design products, digital integrated circuits.

VHDL models capture the essential design information of digital systems, subsystems, and components. The VHDL models, delivered as data items, provide the essential design data needed for future reprocurment of digital electronic devices and systems. These models can also serve to baseline future system modifications. In order that VHDL models satisfy these requirements, both for system development and later for system maintenance and support, it is necessary that models be complete and accurate characterizations of the system or component they represent. In order that they can provide information for future reprocurement or system upgrades, the models must also be processable by future VHDL tools. To assure the models will be compatible with future VHDL tools, the current model development and the future tools must be based on the same standard or one that is maintained so that "upward compatibility"[1] is preserved. (Reference paragraph 2.7.)

3.1.1 Requirements for Testing VHDL Models

In order to assure that delivered VHDL model data items will fulfill future needs for component and subsystem reprocurements or modifications, they first must contain the required information to completely characterize the component or subsystem they represent. The specific data requirements must be contained in the contract data item description (DID) requirements for VHDL models or other contract documented requirements (Reference paragraph 2.4.2).

Secondly, to maximize the assurance the models can be used in the future when the data is needed for system reprocurements, modifications, or upgrades, the VHDL models must be in compliance with the current VHDL Standard. There is an inclination for hardware designers to feel that modeling and models are adequate when the modeling and design process results in a satisfactory component or system function. These designers feel that if a modeling process produces "good silicon," then the model and the tools used in the process must also be "good." This is a logical argument if the modeling process were not to also serve as the documentation resource and the reuse of the models in the future. Because of this requirement, which applies almost universally in DoD system acquisitions, it is necessary that models be developed to comply with the VHDL Standard.

To assure compliance with contract provisions and with the VHDL Standard, VHDL models must be inspected and tested against specific acceptance and verification criteria and procedures. These procedures include model evaluation for compliance with the VHDL DID and other contract provisions, and inspection and testing of the code for VHDL Standard compliance.

Rome Laboratory developed a VHDL Model Verification and Acceptance Procedure. [2] The procedure includes visual inspection, code analysis for conformance with VHDL IEEE 1076, detailed inspection of VHDL modules, and testing and analysis of VHDL simulation models. The visual inspection step determines if all required deliverables are present. A fully compliant VHDL IEEE 1076 analyzer or compiler is used to confirm VHDL model code compliance.[3] The detailed inspection involves technical analysis of required code elements, code comments, model structural, behavioral, and data flow architectures, and testbench coverage. The models are processed by a compliant VHDL simulator to determine final compliance.

3.1.2 Organization Requirements for VHDL Model Testing

Contractors who develop digital systems, subsystems, and components have a responsibility to deliver their products and data as required. However, the weapon system acquisition and support programs are ultimately responsible for assuring that delivered data, including VHDL models, are provided in accordance with contract requirements. Testing responsibilities may be delegated or contracted to other organizations such as the developing contractor's independent validation team, a separate contractor, or another government organization. The VHDL model verification process is similar to other verification functions required in the system acquisition process. They may be done in house, delegated to another government organization, or done by contracted resources.

Currently, there are only a few programs with large VHDL applications. The F-22 Program has contracted for VHDL model verification with an independent contractor. Since there were no validated VHDL tools, the F-22 Program and its testing contractor developed a unique verification process that mitigates the lack of validated VHDL tools.[4] This process appears to be satisfactory as a workaround in the absence of validated tools.

When validated tools become available the model validation process may be simpler, but the need to rigorously test and check conformity will remain. In general, acquiring organizations will not have, or desire to obtain, in-house resources to verify and validate VHDL data. There will always be a need for support in this area, just as there is now in testing for compliance with CALS requirements for text and graphics data .

The AFCTB performs testing to determine compliance with MIL-STD-1840 and associated standards for text and graphics. Data developers and acquisition offices submit digital data to the test bed for testing. The AFCTB also assists data submitters in understanding and complying with CALS data requirements. The AFCTB could develop and provide a similar capability providing VHDL model testing for compliance with ANSI/IEEE 1076 VHDL.

3.2 VHDL Tool Validation/Certification

Various software tools are used in the development of VHDL digital circuit and system models. Other software tools process VHDL model data and develop information to drive the manufacturing process of the digital component end items, i.e., integrated circuits. These tools perform various functions in the model development and circuit manufacture processes. Compilers and analyzers validate the model code. Simulators provide an analysis and prediction of the behavior of circuit and system models. Synthesis tools interpret the VHDL models and synthesize digital logic gate structures which in turn are used in the manufacture of digital elements.

The objective of VHDL tool validation and certification is to achieve standardization of the tools, that is, to be in compliance with the VHDL Standard. In order to assure uniformity across all tools, each tool must be uniformly tested and validated.

3.2.1 Requirements for Testing, Validating/Certifying VHDL Tools

Digital model standardization is necessary so that models can be transported across different tools, a requirement in today's complex electrical design environment. In order to be able to transport models between different tools, the tools must be standard. Different tools designed to perform the same process in model development, a compiler or simulator for instance, must each provide the same results when processing the same model data. In order to assure this, all tools must be developed in accordance with the requirements of the IEEE Standard 1076 VHDL LRM, and then be validated by a single test suite that checks for conformance with all of the Standard's requirements.

3.2.2 Candidate Tool Testing Organizations

Several organizations, both private and in Government, have a stake in assuring tool conformity to the VHDL Standard. There are those who are only concerned that the end product models are standard, and thus their concern is that the models were developed and tested on compliant tools. Other organizations, such as NIST, may be chartered to perform tool testing and validation. The roles and responsibilities of candidate tool testing organizations are discussed in the following paragraphs.

3.2.2.1 VHSIC Program Office

VHDL development was sponsored by the DoD VHSIC Program Office. The purpose of its development was to assist, actually enable, the realization of the full potential of VHSIC technology. Responsibility for the language was turned over the IEEE. The VHSIC Program Office mission is technology development, i.e., future VHSIC improvement, and if appropriate, VHDL improvement. The VHSIC Program Office is not a candidate for VHDL tool testing.

3.2.2.2 Institute of Electrical and Electronic Engineers

The IEEE Computer Society and its subcommittee which is responsible for the VHDL Specification do not have any interest in establishing or maintaining a VHDL validation capability. Their interest is clearly in establishing appropriate standards and maintaining them. However, it is very important that a close working relationship be created and maintained between the VHDL verification organizations/facilities and the IEEE organization that continues to maintain IEEE 1076 VHDL Standard.

3.2.2.3 National Institute of Standards and Technology

The National Institute of Standards and Technology is responsible for improving the utilization and management of computer systems in the Federal Government. NIST coordinates Government efforts in the development of information technology standards and guidelines, and provides validation testing for standards conformance. The NIST Computer Systems Laboratory tests information technology products to determine the degree to which they conform to specific Federal Information Processing Standards. These standards include COBOL, Fortran, Pascal, Ada, and C programming languages.

In June 1992, NIST FIPS PUB 172 announced the adoption of ANSI/IEEE 1076-1987 VHDL. (Reference paragraph 2.4.5) Although VHDL is not a "programming" language, the NIST Computer Systems Laboratory is responsible for FIPS PUB 172 interpretation and for resolution of questions regarding VHDL specifications and requirements. FIPS PUB 172 also directs that NIST is to validate VHDL processors for conformance to the VHDL Standard when validation procedures become available.

NIST is not funded to accomplish the required efforts to develop VHDL validation test tools and validation procedures. The Computer Systems Laboratory relies on "customers" to pay for products and services rendered. NIST anticipates external support to obtain or develop the test tools and procedures to carry out the responsibilities outlined in FIPS PUB 172. The CALS program provides some support for this effort.[5] NIST has not undertaken any effort to plan or to secure funding for a VHDL test capability.

Notwithstanding the lack of current planning or funding, NIST has a responsibility to test VHDL processors, i.e., compilers, simulators, etc. If it is able to secure funding to develop, or is able to obtain a VHDL tool test suite, NIST will provide testing and certification of VHDL tools as it does for most programming languages.

3.2.2.4 Commercial Vendors

Most vendors endeavor to develop their tools in accordance with the VHDL Standard; however, they may not always completely follow all of the details of the Standard. Because of differences in the interpretation of the Standard, tools developed by different vendors may not conform to a particular requirement in the same manner. In other instances, vendors may choose to implement subsets of the Standard's requirements, or vendors may implement "extensions" to the Standard's requirements.

A group of EDA vendors is seeking to develop a test suite which will assist them in developing tools that are uniformly compliant to the Standard. This is discussed in paragraph 4.4. The industry consortium, that is sponsoring the test suite development, is a possible candidate to conduct verification testing of vendor tools when the test suite is fully developed.

3.2.2.5 DoD Programs and Other Users

The program offices or other users, for which VHDL models are developed, are ultimately responsibility for assuring that the models are adequate and satisfy their requirements. As important as it is that system program offices employ validated tools, it is not likely that they will, themselves, be in a position to validate tools used for their developments. When validation capabilities do become available, program offices will require their developers to use validated tools. Program offices and other users will rely on the validation certification of the tool developer or a third party "validator."

3.2.2.6 SM-ALC VHDL Program Office

The AFVPO at the SM/ALC is a candidate VHDL tool testing organization. (Reference paragraph 2.7.2.2.) It provides advanced microelectronics technology support throughout the Air Force. It provides VHDL institutionalization, training development and other related efforts and is a leader in applying VHDL in logistics retrofit engineering. The AFVPO also coordinates with an industry consortium that supports VHDL (Reference paragraph 4.4.1).

3.2.2.7 Air Force CALS Test Bed

In addition to testing data for CALS conformance, the AFCTB currently evaluates commercial tools that support CALS specifications and standards. Commercial tool documentation is reviewed and the tools are tested and evaluated with respect to their advertised capabilities and their functional ability to support CALS specifications and standards. The results of the tool evaluations are used in recommending tools to CALS users. The AFCTB has computer work stations and other computer resources that would lend their support to VHDL tool testing.

3.3 Paradigms of Standards Compliance Testing

As stated earlier, NIST provides testing services for information technology products. NIST tests and certifies COBOL and Fortran computer language compilers. It is one of the two Ada validation facilities in the United States. Additionally, NIST is responsible for testing

tools that support CALS military specifications: Standard Generalized Markup Language (SGML) and Initial Graphic Exchange Specification (IGES).

There are, in addition to the AFCTB, other Air Force organizations that carry out validation and compliance testing similar to the testing required for VHDL. The development and functions of representative capabilities are discussed in the following paragraphs.

3.3.1 Ada Language Compiler Validation

Following the DoD development of the Ada computer language, the DoD developed the capability to test and validate Ada compilers. The development of the Ada compiler validation suite evolved over a period of several years as the Ada language matured. Initially the Ada validation suite tested only selected user-most-needed compiler capabilities and general "pitfall" problems. Each year as many as 600 tests were added as the test suite gradually matured. The current test suite has about 4000 tests. Ada validation is not a stand alone test of an Ada compiler tool by itself, but a validation process involving a combined compiler-host implementation. Certification is given to a specific compiler/host computer/operating system implementation.

The first validation facility, the Air Force Ada Validation Facility (AVF) at Wright-Patterson AFB, OH, began operation in 1985, a year after the last major revision of the Ada Specification. Currently, there are five AVFs throughout the world--in the United Kingdom, France, Germany, and in the United States NIST (DoC) and Air Force (DoD) facilities. Each uses the same validation suite and the validations of each facility are recognized by the others.

During the AVF's busiest time, 3 to 9 implementations were validated per month, the maximum occurring after a new test suite was issued. The introduction of each new test suite requires that all existing compiler implementations be re-validated to assure that they complied with all of the requirements of the Ada standard verified by the newest test suite. New suites were created almost annually in the early years, 1985 to 1989. Only about nine validations are requested per year since the test suite was frozen in 1989.

The validation of an Ada compiler implementation requires about one month of presite effort at the AVF followed by about two weeks on-site, i.e., at the user's facility. At the conclusion of successful site tests, validation certification is issued. A Validation Summary Report is provided which provides guidance in the use of the compiler from the tester's point of view. The cost to validate a compiler implementation by the AF AVF is about $15,000.

Industry is willing to pay to have their Ada implementations validated because the certification is recognized by their customers. Additionally, the NIST FIPS states that Ada programs developed for the Federal Government application must be developed by certified facilities and tools. The industry has come to expect and require that Ada based software products be developed on certified Ada implementations to assure the products are transportable to other certified implementations.

The Ada experience has found that cooperation between the standard controlling agency and the validation agency is very desirable. The responsiveness of both to the needs of the using community has been a key factor in the success of the Ada validation capabilities. Both have been driven by the belief in the need for conformance to a standard, and standardization that meets users needs.

In summary, the Ada language paradigm indicates that validation suites are not necessarily quickly developed, nor must they be totally complete when first used as a certification tool. As the validation suite is upgraded or expanded to cover additional parts of a standards requirements, revalidation of already-validated tools must be accomplished. More than one validation facility may exist, but each must use the same validation suite. This comes in part from the "internationalization" of standards such as Ada. VHDL also falls into this category. The validation of Ada compiler implementations has been successful due to the maturity of the Ada language specification, i.e., the specification has not been changed for ten years.

3.3.2 Other Standards Compliance Testing Examples

There are examples, in addition to the AVF, where the Air Force has taken a lead in digital testing. One that stands out is the conformance testing for the MIL-STD-1750 Instruction Set Architecture Standard. This was done by an Aeronautical Systems Center Avionics Engineering Directorate (ASC/ENA) in house facility. It served as the qualifying agency for hardware developers of this embedded computer hardware/firmware.

NOTES:

1. VHDL Standard "upward compatibility" is defined as the attribute that models developed in accordance with the standard will be compatible and run on tools that comply with later versions of the standard.

2. VHDL Model Verification and Acceptance Procedure, Version 1.0, Rome Laboratory/ERDD, Griffiss AFB, NY, undated.

3. It should be noted that currently there are no validated VHDL analyzers, or other validated tools, available today. This requirement must be met with some work around process, such as selecting a tool or a combination of tools as representing a validated tool.

4. See paragraph 2.5.1 for additional description of the problems encountered because of the lack of standardization and validated tools.

5. The CALS Program, through the AF VHDL Program Office, SM-ALC/TIEFB, has funded a low level NIST effort to update the FIPS PUB 172 to the updated ANSI/IEEE 1076 VHDL Standard.

SECTION IV

VHDL TOOL VALIDATION/COMPLIANCE TEST SUITE DEVELOPMENT

The DoD VHSIC program had made a large investment in the VHDL language development prior to 1985 when it secured the IEEE to sponsor the maintenance of the VHDL Standard. Since that time the IEEE, through its voluntary committees and with Government sponsored support, has developed the VHDL LRM into an acceptable standard. The language has gained wide acceptance and a number of vendors have developed tools to support its application. The VHDL language and the tools that exist today serve the design community quite well, with one major exception--the lack of tool consistency which prevents transporting VHDL models between different vendors' tool sets.

Notwithstanding the progress made in the development and application of VHDL, validation capabilities are not available to test VHDL tools for compliance to the VHDL Standard, nor is there a tool to test VHDL models compliance. Currently, each VHDL tool vendor has its own set of tests to check out its products as they are developed. Each developer interprets the Standard, and adds to or subtracts from its requirements, as tools are designed. The result is, as stated above, the inability to transport models between different vendors' tools. As long as this situation exists, the full capability and benefit of VHDL will not be realized. Without the adherence to the Standard, VHDL will not provide industry or the DoD the capability to use archived VHDL models to reprocure components and subsystems.

Paragraphs 4.1 and 4.2 describe the background and early development of VHDL validation resources. Paragraph 4.3 outlines the responsibilities and goals of the NIST with respect to testing VHDL tools. Paragraph 4.4 describes the effort being put forth by an industry consortium, VHDL International (VI), to develop a VHDL tool validation test suite.

4.1 VHSIC Program VHDL Test Development

The VHDL development was managed by the Electronic Technology Division, Air Force Wright Aeronautical Laboratory. During the development of the VHDL language, rudimentary VHDL compiler and simulator functions were developed to validate the VHDL language structure as it was being defined. Early VHDL tools were tested as they were built to assure that they targeted the language as it was being developed. These test scenarios were never fully developed into formal procedures to test mature VHDL tools. However, an effort was made to gather together and document the various test procedures developed by the VHDL Program contractors. This effort was done by the Virginia Polytechnic Institute (VPI) for the VHSIC Program. The results of the effort were provided to the VHDL community.

4.2 Virginia Polytechnic University VHDL Validation Suite

A group of VHDL tool developers [1] initiated a project in 1988 with VPI to develop a comprehensive VHDL validation suite. VPI developed and documented a formal test suite development process [2]. VPI analyzed the VHDL LRM, documented 1,187 VHDL language syntactic and semantic rules, and defined 2,099 test points covering the syntactic and semantic rules derived from the LRM [3]. Additionally, one or more test objectives were developed to specifically define how each test point was to be tested.

The participating companies provided test cases which they had developed for their own use. VPI evaluated these tests, formatted them to satisfy the defined test point requirements, and developed a test suite that covered about 76 percent of the test points. VPI developed the remaining tests to cover 100 percent of the test points. The test suite was distributed to many electronic design and vendor firms in addition to the six companies that supported the development, to a number of universities, and to a few overseas industries and universities.

The sponsoring firms tested the VPI test suite by using it to test their tools. There was not uniform acceptance of the test suite among the initial users because of differences in which they had interpreted the VHDL LRM. A few vendors' tools failed particular tests, where other vendors' tools passed those same tests. Some conflicts were resolved and those that were not resolved were turned over to the IEEE VASG for resolution.

In addition to the unresolved issues over language rules and test interpretations, the test suite lacked in other aspects. The test suite did not provide tests that covered problem areas where compiler and simulator developers may not be careful in strictly observing the rules of the Standard. Some developers add functions to their tools that are not defined or allowed by the rules of the Standard. The VPI test suite did not check for these types of violations.

4.3 NIST Processor Validation Procedures

NIST responsibilities for VHDL tool validation are articulated in FIPS PUB 172 and are discussed in paragraph 3.2.2.3. FIPS PUB 172 states that NIST is to investigate methods which may be considered for validating VHDL processors. NIST planning includes two tasks. First, the FIPS PUB 172 is to be revised to conform with the updated IEEE VHDL Standard. This task is a one year effort because of the required review and coordination by Federal agencies and affected industries.

The second task is to develop a test suite that conforms to the new FIPS PUB and establish validation procedures. This effort includes: (1) writing test requirements based on the new VHDL Standard; (2) developing the tests/building the test suite; (3) setting up the policies and procedures for the NIST VHDL validation service; and (4) announcing the program and responding to comments before invoking the process. These efforts, according to NIST, will require one to two years, depending on the test suite resources (such as from VPI, or the industry development that is described in the next section) that NIST can obtain to fold into their effort.

NIST does not have funding support to compete these efforts. They may wait until the industry effort, described in the next paragraph, develops the required validation test suit and then try to acquire it.

4.4 VHDL International Test Suite Development

Today, there are more than a dozen EDA vendors who supply VHDL simulation tools and at least half that many already offer synthesis tools. Additionally, up to 40 firms provide other VHDL related products. Some vendors claim their tools are in full compliance with the language standard. Other vendors define a useful subset of the language that their tools comply with. Experienced users of these tools know that the differences between vendors in their interpretation of the language are a source of frustration.

Such differences mean there is little benefit of having multiple tool vendors when each vendor's tool set is unique. Some believe that industry will come together and eventually the differences will be resolved. The IEEE provides a forum for the interpretation and resolution of these problems, but only after they are brought to their attention. Currently this is not being done, since there is no testing agency. The IEEE does not operate as a testing or certifying agency.

To speed up the uniform application of VHDL, the industry consortium, VHDL International, initiated an effort in early 1993 to develop a simulator test suite. The leadership of VI, top executives in EDA firms, felt the need for enforcement of the VHDL standard in marketing VHDL tools. They desire to be able to screen out non-compliant tools. The VI test suite will evolve a set of tests that will allow a user or vendor to verify compliance with the language specification. The test suite will set a mutually agreed-upon target for all tool vendors.

4.4.1 VHDL International Background

VI was founded by six member industries in June 1991 to cooperatively and proactively promote VHDL as the standard worldwide language for the design and description of electronic systems. [4] At least another 20 corporate members have joined and approximately 2600 people hold individual member status. Most of the firms that supported the earlier VPI test suite development are members of VI.

In addition to promoting the use of VHDL, VI provides information to VHDL users, supports and facilitates VHDL organizational efforts, and coordinates and funds on-going activities to support and advance the language. The organization provides the IEEE, and other standards organizations, with recommendations and favorable solutions to user core issues such as model availability, tool interoperability, methodologies, verification compliance, and education.

VI has successfully supported the bi-annual VHDL International Users' Forum (VIUF) conferences over the last several years. VI sponsors 10 established users' groups. VI has a number of working subcommittees, including a DoD Interface Committee.

4.4.2 Initial Test Suite Development Program

VI initiated an effort in early 1993 to develop a test suite which will test VHDL simulators against the current ANSI/IEEE 1076-1987 Standard. The initial effort involves consolidating and reformatting existing test cases in a package that can be easily run against simulators. The test cases are being collected from several sources including (1) test cases developed for the DoD during the VHDL language development, (2) test cases assembled or generated by VPI, (3) tests from the public domain, (4) test cases that may be contributed by vendors, and (5) test cases that may be contributed by users who have developed them during their independent evaluations of vendor products.

4.4.2.1 Initial Test Suite Capability

It is anticipated that the initial test suite will reveal most of the seriously deficient compilers and simulators with respect to not fully mechanizing the VHDL Standard. The capability of the initial test suite is projected by VI as a "first-pass" validation suite that will provide a "sanity check" and a "measure of confidence" in evaluating VHDL simulators. It should flag those tools, especially simulators, that have caused a majority of the problems in the industry because they omitted significant aspects of the Standard. VI management considers the initial test suite could be applied as a validation tool to expose the bad vendor products and encourage developers market compliant products.

The initial test suite will not test for unique mechanizations and other attributes not permitted by the standard. Thus, it may pass tools that are not completely in compliance with the VHDL Standard. Nevertheless it is a first step to a complete testing capability.

4.4.2.2 Initial Test Suite Cost and Funding

The initial effort is a $120K effort contracted to VHDL Consulting Group, Allentown, PA. This company has a good reputation throughout the VHDL and EDA technical communities. Six VI-member companies are financing this effort. The work got underway in April 1993, and is expected to be completed by March 1994.

4.4.3 Follow-on Development Plans

VI is seeking additional support to update and extend the test suite capability, to cover the requirements of the new updated IEEE 1076 VHDL Standard, and to be a credible VHDL simulator validation and certification tool. The first task is to extend the suite's capability to test against the 1993 version of the VHDL Specification. The revision to IEEE 1076-1987 is significant. It will take a considerable effort to define and implement the added tests necessary to cover the new IEEE 1076-1993 VHDL Standard.

In addition, new test cases should be added in "problem areas." These are described as point tests in the most frequently observed problem areas where compiler and simulator developers may not be careful in strictly observing the rules of the Standard. Some problem areas are already known through the experience gained using current simulators. Others will be "discovered" as the initial test suit is exercised.

4.4.3.1 Capability of Follow-on Development

The quality or capability of the validation suite resulting from the planned update effort, described above, can be discussed in terms of a comparison drawn to the Ada programming language compiler validation suite and its development. The Ada validation suite development took several years of iterative development to reach the point where it is now. It can be considered as having a near 100 percent validation capability.

The VHDL suite product development effort of two to three years will not equal the quality of the current Ada compiler validation suite's capability. However, it is considered within reason that the planned VHDL validation suite may have a 98 percent validation coverage. That is to say, it will still miss some non-compliant VHDL simulator characteristics and allow a non-compliant VHDL tool to "pass" validation testing.

4.4.3.2 Cost and Schedule of Follow-on Development

The cost of the update and expansion of the test suite as described above has not been determined. An estimate was offered--an additional $300K to $400K. A total investment of $500K, including the initial $120K, may be required. VI suggested that a more accurate estimate of the effort could be made after the new Standard is established, and a proposal to update the test suite is received from VHDL Consulting Group (and possibly other sources). VI has not developed a schedule for this effort.

An added footnote to cost and schedule of VHDL tool test suite developments: The Ada compiler test suite, with near 100 percent coverage, cost and estimated $20M. VI suggested that a 100 percent VHDL tool validation suite might cost between $5M to $10M. This estimate takes into consideration that the VHDL suite development would be more difficult, but that the development process would be more efficient now than with Ada. However, that VHDL test suite capability and cost is not being considered at this time.

4.4.3.3 DoD Support of Follow-on Development

VI has indicated that it is hopeful that the DoD, specifically the Air Force, will substantially support the second phase of the validation suite development, i.e., $300K to $400K. VI has discussed its plans with the AFVPO. Discussing this expectation, VI reasons that the Government has already spent perhaps as much as $40M on VHDL, developing it to the point where industry has generally accepted the Standard. The reasoning continues that much of the potential value of VHDL to the DoD services can be obtained only when VHDL model

development strictly follows the Standard in a uniform manner. The best way to assure Standard compliance is to require the use of certified tools. This can only take place after validation tools are available to test and certify VHDL model production tools.

Notes:

1. CAD Language Systems, Inc., Dazix, GenRad, MCC, Silicon Compiler Systems, Vantage Analysis, and ZYCAD.

2. VHDL Validation Suite Test Development Manual

3. VHDL Validation Suite LRM Test Points, 25 October 1990 (Revised)

4. Much of the information in this section concerning VI and their involvement with a VHDL tool test suite development was obtained by personal contact with three VI managers, Hillel Ofek, President of VI, Michael Carroll, past President of VI, and David Coelho, Project Engineer for the VI VHDL tool test suite development. David Coelho is also the Executive Vice President of Vantage Analysis Systems. He is a leader in VHDL technology and the author of at least two text/reference books on the subject.

SECTION V

VHDL TOOL VALIDATION FACILITY REQUIREMENTS AND CANDIDATE TEST ORGANIZATIONS

This section describes the assets required to conduct VHDL tool testing, and the capabilities of several candidate organizations to perform the mission and functions of VHDL tool validation.

5.1 Facility Requirements

VHDL tool test facility requirements depend on the scope of the involved organization's testing needs. If the intent is to test only a limited variety of tools, such as a single vendor testing only his own products, the requirements are less extensive than for a facility that is to test all tool products from several vendors. Additionally, the software and potentially the hardware assets of a test facility depend on the range of tools to be tested.

5.1.1 Hardware Requirements

VHDL tools are hosted on all classes of computer equipment--personnel computers (PCs), work stations, and main frame systems. Some VHDL tools are available in several configurations for hosting on different computer resources. Each VHDL tool configuration must be tested individually, residing on its host resource. Thus a versatile VHDL tool test facility will require several of the more popular computer host hardware and software configurations, in order to test most of the tool configurations developed by the EDA industry.

5.1.2 Software Requirements

Unique test software is required to test and validate VHDL tools. This software, the "VHDL tool test suite" is described in Section IV. The test suite provides tests that cover each of the rules of the ANSI/IEEE 1076 VHDL Standard that a tool or set of tools must be in compliance with. The test suite "exercises" the VHDL tool under test by inputting specific code constructs or instructions and comparing the output with the expected (acceptable) output responses. Each type of VHDL tool requires a particular set of test resources. VHDL test suites may be designed and developed to test a specific tool type, such as VHDL code compilers and analyzers, or simulators.

As pointed out in Section IV, a test suite has not been developed as yet to completely test any VHDL tools. Section IV discussed previous development efforts of test tools, and described the current industry consortium effort to develop a test suite that will be able to validate VHDL simulators. The VI consortium is spearheading the development of a VHDL simulator test suite. Currently, this is the only visible test tool development effort. It is not clear at this time when this development will result in a mature test suite. It is also not clear who will have access to this resource. Reference paragraph 5.2.1.

Additional software requirements include basic operating system software and utilities, UNIX, DOS, Windows, etc., for the various hardware environments of the facility.

5.1.3 Personnel Requirements

VHDL tool testing requires engineering and computer science personnel. These personnel require experience with software development and testing. They also need to have a background in digital system design using VHDL modeling and simulation tools.

5.2 Candidate Organization Capabilities

The following paragraphs discuss five organizations/entities that have a potential interest or a capability to participate in VHDL tool testing, validation, or certification.

5.2.1 VHDL International

The industry consortium, VHDL International, is postured for a leading role in VHDL testing. As described earlier, it currently is pursuing the only visible development of a test suite. Other smaller efforts have occurred in the past, but this is the only ongoing work to develop a test suite that may be able to validate VHDL tools for compliance with the VHDL Standard.

Leaders of VI have indicated that their intent is to provide the initial test suite assets to their industry members. First releases will be to test and evaluate the test suite product. Later these member firms will be able to use the test suite to assist in the development and test of their VHDL tool products. It is not clear if the consortium has plans to broaden the availability of the test suite to firms or agencies that are not VI members.

VI could develop or sponsor and support a VHDL tool testing enterprise if another agency does not take an effective leadership role in certifying VHDL tools.

5.2.2 Industry Vendors/Users

Paragraphs 3.2.2.4 and 3.2.2.5 discussed tool validation requirements of commercial tool vendors and users. As described in the preceding paragraph, vendors who are a part of the VI consortium will have access to a test suite that will satisfy their tool development testing needs. The consortium may rent or sell the test suite to tool developers that are not VI members.

As indicated earlier in this report, it is not likely that DoD programs or the electronic designers will develop capabilities to test vendor developed VHDL tools used in their digital system developments. Rather these users will depend on vendor testing and vendor claims, and if available an independent validation and certification, such as by NIST or by a CALS test facility.

5.2.3 NIST Computer Systems Laboratory

The NIST Computer Systems Laboratory is designated to validate VHDL processors. This organization currently provides testing of Fortran, COBOL, GOSSIP, and other computer software tools for conformance with their standards. NIST is one of two Ada validation agents in the United States. NIST is also responsible for conformance testing IGES and SGML tools; however, it has not been funded to develop or acquire a capability to test the tools associated with either of these CALS standards. As was indicated earlier in this report, NIST does not have resources to develop VHDL tool testing assets.

NIST has the basic resources and experience to implement a VHDL tool test capability if it could obtain the VHDL tool test software. When NIST is able to obtain the required VHDL test suite software, it is anticipated that it will become a VHDL tool test and certification agency.

5.2.4 SM-ALC Advanced Electronic Technology Group

Paragraphs 2.5.2 and 3.2.2.6 discussed the VHDL activities of the SM-ALC AETG. The AETG has many of the hardware resources, as well as a cadre of personnel with VHDL application experience, to support a VHDL tool test capability. The AFVPO is considering support of the VI test suite development with CALS resources. If CALS supports the VI test suite development and obtains access to the test suite, AETG is a prime candidate facility for VHDL tool testing, validation, and certification.

5.2.5 Air Force CALS Test Bed

The AFCTB is a possible candidate to perform VHDL tool testing and validation. The major thrust of the AFCTB is testing CALS data compliance. In doing this testing the AFCTB has conducted evaluations of several software tools associated with preparing CALS compliant data. CALS software tool evaluations continue as new tools are acquired or provided by vendors for evaluation. These evaluations are not validation tests in the strictest sense. The CALS Program has not felt the need to do strict validation testing of the tools used to develop CALS data, i.e., SGML, IGES, raster, etc., tools. Strict software tool compliance with respect to these CALS data requirements has not been considered as critical as it is in the case of VHDL tool compliance.

The AFCTB has the basic host hardware and software required for a VHDL tool validation test capability. Currently, test bed personnel do not have specific VHDL experience; however, the past experience in tool evaluation and in data testing provides an excellent background for VHDL testing. As VHDL test suite assets become available, AFCTB personnel can become familiar with VHDL requirements, and develop a test and validation capability for both VHDL tools and data. (See paragraph 6.2.4.)

SECTION VI

VHDL DATA TESTING FACILITY REQUIREMENTS AND CANDIDATE ORGANIZATION CAPABILITIES

This section discusses the assets required to conduct VHDL data testing and candidate organization capabilities to perform VHDL data validation. VHDL data consists of VHDL models of digital systems, subsystems, and components. Modeling is done at all system design levels from high level architecture models, which portray specification level requiremens, to gate level models, which interface with integrated circuit manufacturing software.

The requirements and philosophy of VHDL data testing were discussed in Section III. Testing models for compliance with the VHDL Standard is part of the model data verification and acceptance procedures described in paragraph 3.1.1. Testing model data for VHDL Standard compliance is essentially determining that the data can be processed by VHDL Standard compliant compilers, analyzers, or simulators. Model data compliance with the VHDL Standard maximizes the assurance that models can be used in the future when the data is needed for system reprocurements, modifications, or upgrades.

It was noted in Section III, that as the digital design and development process is carried out, the design products--the manufactured integrated circuits--can validate the modeling process. That is the circuit products validate the development process, including the VHDL modeling, when the circuits perform under test or actual operation as specified and required. Thus, if VHDL compliant tools are used in the total design process from high level system architecture to gate level modeling, then separate model data testing for VHDL compliance may be redundant.

VHDL model data may be tested independently of the design process at any or all levels of design. Independent confirmation of VHDL model data is a part of system design and development acceptance procedures described in paragraph 3.1.1. Subsection 6.1 that follows outlines facility, computer resources, and personnel requirements for data testing. Subsection 6.2 discusses several organizations that could implement a capability to test VHDL model data for compliance with ANSI/IEEE 1076.

6.1 Facility Requirements

VHDL data test facility requirements depend on the extent of the data validation to be accomplished. Simple code checking requires only a hosted VHDL compliant compiler or analyzer. Determining if models are simulatable or sufficient for circuit synthesis requires simulator and synthesis software tools and the hardware to support them.

6.1.1 Computer Resource Requirements

VHDL model data testing requires the same VHDL tools that are involved in the model development process, i.e., compilers, analyzers, simulators and synthesizers. As indicated in Section V, these tools are hosted on all types of computers, from PCs to mainframes. A workstation, such as a SUN Sparc, with a UNIX operating system, is sufficient to support the data testing described above. A fully compatible VHDL Standard compliant compiler, analyzer, and simulator complete the required computer resources for basic model testing.

6.1.2 Personnel Requirements

VHDL data testing requires engineering and computer science personnel with software development and test experience. These personnel also require a background or experience in VHDL system design, modeling, simulation, and synthesis tools and processes.

6.2 Candidate Organization Capabilities

Paragraph 3.1.2 discussed the general requirements for data validation of candidate VHDL model testing organizations. This section briefly describes the capabilities of those organizations that could have a role in VHDL data testing.

6.2.1 Industry System/Subsystem/Component Developer

Until validated VHDL Standard compliant tools become available, independent model verification will be needed to increase the assurance that models are in "close compliance" with the Standard. System and component developers have the basic resources to conduct independent tests. They may use a second or third VHDL tool set, apart from the set used to initially develop the models, to test model data, just as the F-22 Program method for conformance testing. (Reference paragraph 2.5.1.3.)

When certified VHDL Standard compliant tools become available and developers begin using them, there may not be a need for a separate check for model data compliance within their organizations. The use of compliant VHDL modeling tools generally will result in compliant model data.

6.2.2 Defense Electronics Supply Center

DESC is tasked to be a repository for VHDL models of digital electronic components. To support this function, DESC is developing the capability to validate model conformance to the VHDL Standard, insofar as is possible at this time without validated tools, and verify that the models are "good" models viable for use in a future reprocurement, or reuse in a new application.

In place of "validated tools'" to do model testing, DESC is employing two of the more widely accepted VHDL tools sets for data testing. These tool sets include compilers and simulators. DESC is also developing a special test capability to verify that models can be synthesized with current available synthesis tools. Synthesis tools are not mature at this time. (Standardization of synthesis technology is addressed for the first time in the IEEE 1076-1993 VHDL Standard update.) DESC is a pioneer in this area.

6.2.3 DoD Acquisition and Support Activities

DoD acquisition and support programs, for the most part, will not acquire VHDL data test capabilities. Rather they will rely on contractor support, much as the F-22 Program currently does, or seek test support from another Government agency that has a data testing capability such as SM-ALC AETG, or the AFCTB, if they develop the required test capabilities.

The SM-ALC AETG, and the Air Force VHDL Program Office within that organization, currently have the resources to do VHDL data testing. Their facilities include several VHDL tool sets. They have developed a significant level of experience in VHDL modeling as they have carried out retrofit engineering projects.

6.2.4 Air Force CALS Test Bed

The AFCTB has the basic hardware and software required to begin the development of a VHDL data test capability. It lacks only the VHDL tool suites, i.e., compilers and simulators. Currently, test bed personnel do not have specific VHDL experience; however, the past experience of several years of CALS data testing provides a background for VHDL data testing.

The addition of VHDL data testing services and VHDL tool validation would round out a very capable testing resource for the CALS Program to provide support to DoD programs, in particular Air Force programs. The extent to which the AFCTB could serve the broad spectrum of acquisition and support programs is problematic. However, it would be a valued asset as a service to programs with small VHDL testing needs, and also as a consulting service to other programs as they begin to acquire VHDL data and as they initiate independent testing programs contractually.

SECTION VII

SUMMARY AND CONCLUSIONS

7.1 Summary

Advances in digital integrated circuit technology, brought about largely by the DoD VHSIC program, led to the development of VHDL. This HDL allows circuit designers to efficiently use the full potential of VHSIC and VLSI technologies. VHDL provides designers a full spectrum of digital systems modeling and simulation capabilities from high level design to gate level circuit architectures. VHDL model simulation and testing give designers the ability to accurately predict system operation prior to committing designs to expensive hardware fabrication.

VHDL uniquely supports system acquisition design, maintenance support, and re-procurement of digital systems and components. Its use can greatly reduce acquisition and support costs by eliminating duplicative manual processes. VHDL models of systems provide complete engineering documentation that is invaluable in complex development environments where multiple developers share common system interfaces. VHDL models also provide the engineering design documentation for future reprocurement and retrofit engineering.

Following the initial VHDL development, the DoD VHSIC Program obtained IEEE support to standardize and maintain the language. The ANSI/IEEE 1076-1987 VHDL Standard was approved in 1987. A major update, IEEE 1076-1993, the first revision of the standard, has recently been approved by the IEEE standardization committee process.

VHDL is widely used across industry and has growing industry support. EDA vendors are currently developing and marketing more tools for VHDL than for any other HDL. VHDL is beginning to be applied in the DoD. It is the basis of all the F-22 digital avionics development and it is also being applied as a valuable redesign tool in several maintenance upgrade programs. DoD and Federal guidance requires VHDL application: MIL-STD-454N requires that VHDL be applied in DoD electronic equipment development, and FIPS PUB 172 adopts VHDL as a Federal data processing standard and mandates it use. Additionally, VHDL is cited in MIL-HDBK-59B, identified as a "CALS building block" to acquire intelligent data.

The DoD CALS Program Office has given DESC the responsibility to archive VHDL models at the component level. DESC has developed the capability to receive, test, verify, and archive VHDL component models. The archived models will provide data for future component reprocurements as well as data to support component applications in other system developments. The DoD services are to submit VHDL models of all new or modified components to DESC.

The AFVPO at SM-ALC supports VHDL in a number of ways including training development and application support. It coordinates and supports efforts to formalize Government endorsement and support of the VHDL standard. Support was provided to NIST to update the VHDL FIPS PUB to align it to the IEEE VHDL Standard upgrade. The AFVPO is planning to support the industry consortium VHDL validation suite development.

The AFCTB initiated this study to analyze and document the requirements for VHDL testing, and to determine an appropriate AFCTB involvement in VHDL testing. The study also investigated requirements to support VHDL standardization activities, in particular the development of a VHDL tool validation test suite.

7.2 Findings

Eight major findings listed below lead to the conclusions that follow.

7.2.1 VHDL is Widely Used

The VHDL Standard is enjoying wide support and usage. A variety of software tools have been developed in the EDA community to support the application of VHDL in the design of digital systems and integrated circuit components. Tool vendors continue to increase the number of tools and tool types available to system designers.

7.2.2 VHDL Tools Are Not Uniformly Compliant With the Standard

Compliance to the VHDL Standard is a goal of most tool developers, but in reality most of the tool sets differ from each other. As a result, when two or more system designers use tools from different developers, their design models often cannot be hosted or run on the other designers' tools. This interferes with the sharing of design requirements and design data among developing team members.

7.2.3 Conforming VHDL Tools Are Required to Maximize VHDL Effectiveness During System Design and Development

In order to develop VHDL models that conform to the VHDL Standard, compiler and simulator tools that conform to the VHDL Standard must be used. Models that conform to the VHDL Standard will be compatible across conforming VHDL tools throughout a system design, development, and manufacturing processes. A capability to test and validate VHDL tools is required to realize the potential of VHDL in system design and development.

7.2.4 Conforming VHDL Tools Are Required to Maximize the Assurance That VHDL Models Will Be Usable for Future Reprocurement and Redesign

Model validation to conformance with the VHDL Standard maximizes the assurance that models will be usable on VHDL validated tools in future reprocurement or system upgrades. VHDL compiler and simulator tools, validated as conforming to the VHDL Standard are

required to develop, test, and validate VHDL models. A capability to test and validate VHDL tools is required to achieve the fullest potential of VHDL to serve future reprocurement and redesign of systems and components.

7.2.5 There Are No VHDL Tool Validation Capabilities Available

Tools and procedures to test and validate VHDL have not been developed. The design industry, tool vendors, and the standards community do not have the capability to validate VHDL tools with respect to the accepted VHDL Standard. There are no test suites or test procedures that can test the VHDL tools that are now in use by either the DoD system or commercial product developments, or to test new tools that are being developed by EDA vendors.

Although NIST has the responsibility for validating VHDL tools to be used in Federal government acquisitions, NIST does not have the resources to develop the required validation test suite. There are no DoD efforts to develop a VHDL tool test suite.

7.2.6 A VHDL Tool Test Suite Is Under Development by an Industry Consortium

The industry consortium, VI, is leading an initiative to develop a test suite that can be used to validate VHDL simulators, compilers and analyzers. This industry group sees this as a step to influence all EDA vendors to comply with the ANSI/IEEE 1076 VHDL Standard. The initial phase of this development is under way. VHDL International is looking to the DoD, Air Force, or CALS for support in their tool suite development.

7.2.7 Responsive Tool Validation Services Are Required

When a validation tool suite becomes available, there will be a large demand for VHDL tool testing services. There are a great number of tool installations in use in digital system and electronic circuit design community that should be validated before they are applied to new system developments for the DoD or industry. There will (or should be) a requirement for each of these tools to be validated. As was the case for the validation of Ada tools, more than one validation facility service may be required.

7.2.8 There Is a Need for VHDL Model Validation Services

Model data compliance with the VHDL Standard maximizes the assurance that models can be used in the future when the data is needed for system reprocurements, modifications, or upgrades. Models that are developed using validated VHDL tools can be considered in conformance with the VHDL Standard without additional testing. Nevertheless, there are a number of organizations that may desire to independently validate VHDL models during the development process. In particular an independent confirmation of VHDL model data may be part of system development acceptance procedures.

7.3 Conclusions

Industry is rapidly adopting VHDL as its primary HDL. In the past VHDL has been applied more in commercial applications than in DoD systems. However, DoD agencies are now beginning to apply VHDL to more applications. The number of DoD applications will increase in both the update support of existing systems as well as in new system developments. The application of VHDL in these developments will reduce their costs. Still greater significance exists in the full realization of VHDL potential. Inestimable cost savings will accrue in the future support of digital systems that have been designed and documented with VHDL.

In order to achieve the full potential of VHDL in the development and support of digital electronic systems, it is essential that VHDL be consistently applied as a design and documentation standard throughout the industry. The rules of standardization are contained in the ANSI/IEEE 1076 VHDL Standard. However, in order to uniformly implement that Standard, validated tools must be consistently used across the electronic design arena. A VHDL tool test suite must be developed. Following its development and its own validation, the tool test suite must be applied uniformly to all of the VHDL tool products from all EDA vendors. Until that occurs, each development and support program must assure that the tools applied in its digital system's design have been validated as conforming to the VHDL Standard.

The DoD has made a large investment in the development of VHDL over several years. Currently the DoD is not providing significant resources toward the support of the application and institutionalization of the VHDL standard. There is a need for additional DoD support to expedite the full realization of the potential of VHDL in the DoD as well as in the commercial enterprise.

Although VHDL may provide a larger economic benefit in the commercial sector, there is a still greater significance of the effective application of VHDL standardization in the DoD. DoD weapon systems have long service lifetimes during which the systems, subsystems, and components are reprocured, and redesigned, often several times. It is during these long weapon system life-cycles that the existence of VHDL digital system design data will be of great value to accomplish reprocurement without re-engineering and redesign without re-engineering digital designs. It is necessary that this design data be usable in the EDA tools used in later re-manufacturing and re-design. Standardization is the key.

In order assure standardization and to expedite the full realization of VHDL's potential to the DoD, support is needed to develop and validate the test suite for VHDL tools. Once the VHDL tool test capability is developed, validated, and made available to NIST, and to DoD testing organizations such as the AFCTB. DoD weapon system acquisition and support programs can then require the application of validated tools in the development of digital systems. They will also be able to verify that acceptable VHDL design data is delivered by

their contractors, and have the best assurance that the data will be usable for future support requirements.

The institutionalization of VHDL is important to both economical acquisition and efficient support of digital subsystems of every application, especially to DoD weapons systems.

APPENDIX A

LIST OF ACRONYMS

AETG	Advanced Electronics Technology Group
AFCTB	Air Force CALS Test Bed
AFVPO	Air Force VHDL Program Office
AHDL	Analog Hardware Description Language
ANSI	American National Standards Institute
ASCM	Advanced Spaceborne Computer Module
ASIC	application-specific integrated circuit
ATF	Advanced Tactical Fighter
ATS	automatic test system
AVF	Ada Validation Facility
ASD	Aeronautical Systems Division
CALS	Continuous Acquisition and Life-cycle Support
CEENSS	Continuous Electronics Enhancement Using Simulatable Specifications
CTN	CALS Test Network
DASS	Design Automation Standards Subcommittee
DESC	Defense Electronic Supply Center
DID	data item description
DLA	Defense Logistics Agency
DoC	Department of Commerce
DoD	Department of Defense
EDA	electronic design automation
EDIF	Electronic Design Information Format
FEWS	Forward Electronic Warning System
FIPS	Federal Information Processing Standard
HDL	hardware description language
IEEE	Institute of Electrical and Electronic Engineers
IGES	Initial Graphic Exchange Specification
LH	Light Helicopter
LRM	Language Reference Manual

NIST	National Institute of Standards and Technology
PUB	publication
R&D	research and development
RAF	Royal Air Force
RTL	register transfer logic
SOW	statement of work
SM-ALC	Sacramento Air Logistics Center
SGML	Standard Generalized Markup Language
TDSS	top down system simulation
TISSS	Tester Independent Software Support System
TPS	test program set
UK	United Kingdom
VASG	VHDL Analysis and Standardization Group
VHDL	VHSIC Hardware Description Language
VHSIC	very high speed integrated circuit
VI	VHDL International
VIUF	VHDL International Users' Forum
VLSI	very large scale integration
VPI	Virginia Polytechnic Institute
WAVES	Waveform and Vector Exchange Standard